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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/761,486	01/16/2001	Wen-Chih Chiou	67,200-306	6239

7590 01/03/2003

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EXAMINER	
MARKHAM, WESLEY D	
ART UNIT	PAPER NUMBER
1762	10

DATE MAILED: 01/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/761,486	Applicant(s) CHIOU ET AL.	
	Examin r Wesley D Markham	Art Unit 1762	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2002 and 06 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-7 and 9-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-7 and 9-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *30 September 2002* is: a)☒ approved b)☐ disapproved by the Examiner

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application (i.e., as paper #9 on 11/6/2002) after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/30/2002 (i.e., amendment C, paper #7) has been entered.

Response to Amendment

2. Acknowledgement is made of applicant's amendment C, filed as paper #7 on 9/30/2002, in which a proposed drawing correction was submitted, Claims 3, 4, and 8 were canceled, and Claims 1, 2, 12, 13, and 17 were amended. Claims 1, 2, 5 – 7, and 9 – 17 are currently pending in U.S. Application Serial No. 09/761,486, and an Office Action on the merits follows.

Drawings

3. The proposed drawing correction and/or the proposed substitute sheets of drawings (i.e., 1 sheet containing proposed changes to Figures 4 and 5), filed on 9/30/2002, has been approved. A proper drawing correction or corrected drawings are required

in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

4. The Patent and Trademark Office no longer makes drawing changes. See 1017 O.G. 4. It is applicant's responsibility to ensure that the drawings are corrected. Corrections must be made in accordance with the instructions below.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

Correction of Informalities -- 37 CFR 1.85

New corrected drawings must be filed with the changes incorporated therein. Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the "Notice of Allowability." Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136 for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

Corrections other than Informalities Noted by Draftsperson on form PTO-948.

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

Timing of Corrections

Applicant is required to submit acceptable corrected drawings within the time period set in the Office action. See 37 CFR 1.185(a). Failure to take corrective action within the set (or extended) period will result in **ABANDONMENT** of the application.

Claim Objections

5. The objections to Claims 9 and 12, set forth in paragraphs 5 and 6 of the previous Office Action (i.e., the final Office Action, paper #6, mailed on 7/31/2002), are withdrawn in light of applicant's amendment C.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 5 – 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Specifically, Claims 5 – 7 recite the limitation "said gas" in lines 2 – 3 of each of the claims. There is insufficient antecedent basis for this limitation in the claims. Please note that amended independent Claim 1 (from which Claims 5 – 7 depend) requires annealing the dielectric ARC layer at a temperature of at least 400° C, but no "gas" is recited in the claim. For the purposes of examination only, the examiner has interpreted the "gas" of Claims 5 – 7 to be equivalent to a gas used in the annealing process of Claim 1.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 1, 2, 5, 9 – 11, and 13 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Plat et al. (USPN 6,265,751 B1) in view of Holscher et al. (6,274,292 B1).

12. Regarding independent Claims 1 and 13, Plat et al. teach a method of depositing and condensing an anti-reflective coating (ARC) layer, the method comprising providing a pre-processed semiconductor substrate coated with a polysilicon layer on a top surface (Col.4, lines 35 – 39), depositing a dielectric ARC layer on the polysilicon layer, the dielectric layer typically being SiON (Col.4, lines 38 – 39,

Col.5, lines 45 – 54), and annealing / heating the dielectric ARC layer deposited on the semiconductor substrate at a temperature of between about 400° C and about 1000° C in a gas / environment comprising at least one of N_2 or O_2 (Col.6, lines 59 – 65). Specifically, Plat et al. teach annealing at a temperature between 800 and 900 degrees Fahrenheit (i.e., 427° C to 482° C) in an oxygen gas environment (Col.6, lines 59 – 65). Plat et al. do not explicitly teach that the dielectric ARC layer is either SiO_2 or SiONH. Specifically, Plat et al. teach that a "conventional ARC layer" is provided on the polysilicon layer (Col.2, lines 47 – 49), and that the conventional ARC layer is typically SiON (Col.4, lines 38 – 39). However, the process of Plat et al. does not appear to be limited to solely a SiON ARC layer. Holscher et al. teach the functional equivalence of a SiON dielectric ARC layer (i.e., as taught by Plat et al.) and a SiONH dielectric ARC layer (i.e., as claimed by the applicant) in the art of reducing reflections during the patterning of photoresist layers in semiconductor device applications (Col.2, lines 56 – 65). Therefore, it would have been obvious to one of ordinary skill in the art to substitute a SiONH dielectric ARC layer (i.e., as taught by Holscher et al.) for the SiON dielectric ARC layer in the process of Plat et al. with the reasonable expectation of (1) success, as SiON and SiONH dielectric ARC layers are chemically similar, and (2) obtaining similar results, specifically depositing a conventional ARC layer to a desired thickness on a polysilicon layer and then annealing the ARC layer to densify it, as desired by Plat et al. While the combination of Plat et al. and Holscher et al. presented above does not explicitly teach that the method is used for adjusting the optical properties of an ARC layer

(Claim 1), or for adjusting the extinction coefficient of the ARC layer (Claim 13), the combination of Plat et al. and Holscher et al. teach performing all the process steps / limitations of applicant's independent Claims 1 and 13. Therefore, unless essential process limitations are missing from the applicant's claims, the method of the combination of Plat et al. and Holscher et al. would have inherently adjusted the optical properties, such as the extinction coefficient, of the ARC layer.

13. The combination of Plat et al. and Holscher et al. teaches all the limitations of Claims 2, 5, 9 – 11, and 14 – 17 as set forth above in paragraph 12 and below, including a method wherein / further comprising:

- Claim 2 – The dielectric ARC layer is SiONH (see paragraph 12 above).
- Claim 5 – The gas used in the annealing process is O_2 (Col.6, lines 64 – 65 of Plat et al.).
- Claim 9 – The annealing is performed at a temperature between about 400° C and about 1000° C (Col.6, lines 59 – 65 of Plat et al.).
- Claims 10 - 11 – The annealing is performed for a time period between about 1 minute and about 30 minutes (Claim 10), preferably between about 3 minutes and about 5 minutes (Claim 11) (Col.6, lines 63 – 64 of Plat et al.).
- Claim 14 – The heating is performed for a length of time sufficient to vary the extinction coefficient of the ARC layer by at least 10%. While this limitation is not explicitly taught by the combination of Plat et al. and Holscher et al., Plat et al. do teach performing the applicant's claimed

process at temperatures in the range claimed by the applicant. In addition, Plat et al. teach an annealing time of up to thirty minutes (Col.6, lines 63 – 64), which is the same upper limit for annealing time contemplated by the applicant. Therefore, unless essential process limitations are missing from the applicant's claims, the method of the combination of Plat et al. and Holscher et al. would have inherently varied the extinction coefficient of the ARC layer by at least 10%.

- Claims 15 – 16 – The heating is performed for a length of time between about 1 minute and about 30 minutes, specifically between about 3 minutes and about 5 minutes (Col.6, lines 60 – 65 of Plat et al.).
- Claim 17 – Heating the semiconductor substrate to a temperature between 400° C and 700° C in an environment of O_2 (see paragraph 12 above).

14. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Plat et al. (USPN 6,265,751 B1) in view of Holscher et al. (6,274,292 B1), and in further view of Demirlioglu (USPN 6,063,704).

15. The combination of Plat et al. and Holscher et al. teaches all the limitations of Claim 6 as set forth above in paragraph 12, except for a method wherein the gas used in the annealing process is N_2. Specifically, Plat et al. teach that the gas used in the annealing process can be O_2 (Col.6, lines 64 – 65), but the gas used in the process does not appear to be limited to O_2 alone. In addition and importantly, the annealing process of Plat et al. is designed to densify the dielectric ARC layer (Col.5, lines 45

– 67, and Col.6, lines 59 – 67). Demirlioglu teaches that it was known in the art at the time of the applicant's invention to densify a dielectric ARC layer in a semiconductor device by annealing the layer in an inert ambient such as N_2 (Abstract and Col.8, lines 16 – 26). Therefore, it would have been obvious to one of ordinary skill in the art to utilize N_2 in the annealing process of Plat et al. with the reasonable expectation of successfully densifying the dielectric ARC layer of the combination of Plat et al. and Holscher et al., as desired by Plat et al. and taught by Demirlioglu. In addition, by using an inert gas such as N_2 in the annealing process instead of a flammable gas such as O_2, one of ordinary skill in the art would have obtained the benefit of reducing the risk of fire and explosion in the process, thereby increasing the safety of the process.

16. The combination of Plat et al., Holscher et al., and Demirlioglu teaches all the limitations of Claim 7 as set forth above in paragraphs 12 and 15, except for a method wherein the gas used in the annealing process is a mixture of O_2 and N_2. However, Plat et al. teach annealing in oxygen gas to densify the ARC layer. In addition, it would have been obvious to one of ordinary skill in the art to utilize nitrogen gas in the annealing process to densify the ARC layer for the reasons set forth in paragraph 15 above. Therefore, since one of ordinary skill in the art would have reasonably expected both oxygen and nitrogen to function effectively as the annealing gas in the process of the combination of Plat et al. and Holscher et al., it would have been obvious to one of ordinary skill in the art to use a combination of the two gases with the reasonable expectation of success and obtaining similar

results (i.e., effectively increasing the density of a dielectric ARC layer by annealing the layer, as desired by Plat et al.), absent any showing of criticality or unexpected results obtained by using a mixture of the two gases as opposed to either gas individually.

17. Claims 1, 2, 6, 9 – 11, and 13 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holscher et al. (USPN 6,274,292 B1) in view of Plat et al. (USPN 6,265,751 B1).

18. Regarding independent Claims 1 and 13, Holscher et al. teach a method for adjusing the optical properties / extinction coefficient of a dielectric ARC (Abstract, Col.2, lines 56 – 67, and Col.3, lines 58 – 60), the method comprising providing a preprocessed semiconductor substrate (Col.2, lines 38 – 55), depositing a dielectric ARC layer on the substrate, the ARC layer preferably being either SiON or SiONH (Col.2, lines 56 – 67), and heating / annealing the semiconductor substrate at a temperature of between about 400° C and about 1000° C in an environment / gas which comprises at least one of N_2 or O_2 (Col.3, lines 20 – 37). Holscher et al. do not explicitly teach that the ARC layer is deposited on either a SiN or a polysilicon layer which is provided on the semiconductor substrate. However, it is the intention of Holscher et al. to provide an effective ARC layer that can be used on top of a reflective layer and beneath a photoresist layer to suppress reflected radiation waves from the reflective layer (Col.1, lines 12 – 57). Importantly, Holscher et al. also teach that the semiconductive substrate on which the ARC layer is deposited

includes a semiconductive wafer alone as well as assemblies comprising other materials thereon (Col.2, lines 46 – 55). In other words, the process of Holscher et al. is open to any number of conventionally deposited layers being present between the dielectric ARC layer and the semiconductor substrate. Plat et al. teach that, in conventional semiconductor devices, an ARC layer is deposited on top of a polysilicon layer to reduce reflections, and a photoresist layer is then patterned on top of the SiON ARC layer (Col.1, lines 21 – 35, Col.2, lines 25 – 30 and 47 – 49). Therefore, it would have been obvious to one of ordinary skill in the art to deposit the ARC layer of Holscher et al. on top of a polysilicon layer as taught by Plat et al. with the reasonable expectation of (1) success, as Holscher et al. teach that their ARC layer can be deposited on either a semiconductor substrate or on a substrate with other materials thereon, and (2) obtaining the benefit of reducing the reflections from the polysilicion layer by depositing the ARC layer on the polysilicon layer prior to photoresist processing, as desired by Holscher et al. and taught by Plat et al.

19. The combination of Holscher et al. and Plat et al. also teaches all the limitations of Claims 2, 6, 9 – 11, and 14 – 16 as set forth above in paragraph 18 and below, including a method wherein / further comprising:

    - Claim 2 – The dielectric ARC is SiONH (Col.2, lines 56 – 61, and Col.3, lines 25 – 28 of Holscher et al.).
    - Claim 6 – The gas used in the annealing process is N_2 (Col.3, lines 33 – 37 of Holscher et al.).

- Claim 9 – The annealing is performed at a temperature between about 400° C and about 1000° C (Col.3, lines 20 – 33 of Holscher et al.).
- Claims 10 - 11 – The annealing is performed for a time period between about 1 minute and about 30 minutes, particularly between about 3 minutes and about 5 minutes. Specifically, Holscher et al. are silent as to the annealing time period. However, Holscher et al. teach that the annealing is performed to alter at least one of the refractive index or the extinction coefficient of the ARC layer (Col.3, lines 58 – 60). One of ordinary skill in the art would have readily recognized the annealing time as a result / effective variable that would have been expected to influence the final properties of the ARC layer (i.e., the longer the annealing time, the larger the change in the optical properties of the layer such as refractive index and extinction coefficient). Further, Plat et al. teach that it was known in the art at the time of the applicant's invention to anneal an ARC layer for a time period between approximately 5 and 30 minutes (Col.6, lines 63 – 64). Therefore, it would have been obvious to one of ordinary skill in the art to perform the annealing process of Holscher et al. for a time period of between approximately 5 and 30 minutes (as taught by Plat et al.) with the reasonable expectation of success. Further, absent any showing of criticality or unexpected results, the exact annealing time would have been optimized through routine experimentation by one of ordinary skill in the art,

depending on the desired degree of change in the optical properties of the ARC layer.

- Claim 14 – The heating is performed for a length of time sufficient to vary the extinction coefficient of the ARC layer by at least 10% (Col.3, lines 55 – 60 of Holscher et al.).
- Claims 15 – 16 – The heating is performed for a length of time between about 1 minute and about 30 minutes, specifically between about 3 minutes and about 5 minutes (See bullet for Claims 10 – 11 above).

20. Claims 5, 7, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holscher et al. (USPN 6,274,292 B1) in view of Plat et al. (USPN 6,265,751 B1), and in further view of Sandhu et al. (USPN 6,268,282 B1).
21. The combination of Holscher et al. and Plat et al. teaches all the limitations of Claims 5 and 17 as set forth in paragraph 18 above, except a method wherein the gas / environment used in the annealing process is O_2. However, it is the aim of Holscher et al. to anneal an ARC layer such as a SiONH layer in order to alter at least one of the refractive index or extinction coefficient of the ARC layer (Col.3, lines 58 – 60). Sandhu et al. teach that, when annealing an ARC material in an oxygen environment, the annealing alters the refractive index and the extinction coefficient of the ARC layer (Col.2, lines 35 – 47). Therefore, it would have been obvious to one of ordinary skill in the art to use oxygen as the gas in the annealing process of Holscher et al. with the reasonable expectation of successfully altering at

least one of the refractive index or extinction coefficient of the ARC layer, as desired by Holscher et al. and taught by Sandhu et al.

22. The combination of Holscher et al., Plat et al., and Sandhu et al. teaches all the limitations of Claim 7 as set forth in paragraphs 18 and 21 above, except for a method wherein the gas used in the annealing process is a mixture of O_2 and N_2. However, Holscher et al. teach that the annealing process gas used can comprise nitrogen (Col.3, lines 35 – 37). In addition, it would have been obvious to one of ordinary skill in the art to use oxygen as the gas in the annealing process of Holscher et al. for the reasons set forth in paragraph 21 above. Therefore, since one of ordinary skill in the art would have expected both oxygen and nitrogen to function effectively as the annealing gas in the process of Holscher et al., it would have been obvious to one of ordinary skill in the art to use a combination of the two gases with the reasonable expectation of success and obtaining similar results (i.e., successfully annealing a dielectric ARC layer in order to alter the optical properties thereof), absent any showing of criticality or unexpected results of using a mixture of the two gases as opposed to either gas individually.

23. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Holscher et al. (USPN 6,274,292 B1) in view of Plat et al. (USPN 6,265,751 B1), and in further view of either Lee (USPN 6,300,672 B1) or Yao et al. (USPN 6,258,734 B1).

24. The combination of Holscher et al. and Plat et al. teaches all the limitations of Claim 12 as set forth in paragraph 18 above, except a method wherein the annealing

process adjusts the refractive index of the ARC layer to between about 2.0 and 2.5 and the extinction coefficient to between about 0.2 to 0.8. However, it is the goal of Holscher et al. to adjust the refractive index and the extinction coefficient of a SiONH ARC layer to a desirable value in order to reduce reflections during subsequent photoresist processing. Lee teaches that typical ARC layers used in semiconductor devices during photoresist patterning (i.e., a process analogous to that of both Holscher et al. and Plat et al.) have a refractive index of about 1.60 – 3.6 and an extinction coefficient of about 0.01 – 2.0 (Abstract and Col.5, lines 25 – 31). Yao et al. teach that key characteristics of an ARC layer used in semiconductor devices during photoresist patterning include a refractive index of between about 1.85 and 2.35 and an extinction coefficient of between about 0.45 and 0.75 (Abstract and Col.2, lines 9 – 27). Therefore, it would have been obvious to one of ordinary skill in the art to adjust the refractive index of the ARC layer of the combination of Holscher et al. and Plat et al. to between about 2.0 and 2.5 and the extinction coefficient to between about 0.2 to 0.8 with the reasonable expectation of (1) success, as Holscher et al. teach that the annealing of an ARC layer such as a SiON or SiONH layer alters at least one of the refractive index or extinction coefficient of the ARC layer, and (2) obtaining the respective refractive index and extinction coefficient values for the ARC layer that are desired in the art, as taught by either Lee or Yao et al.

Response to Arguments

25. Applicant's arguments filed on 9/30/2002 have been fully considered but they are not persuasive.

26. First, regarding the applicant's arguments drawn to the Plat et al. and Abernathey et al. references, these arguments are moot in view of the new grounds of rejection presented above.

27. Second, the applicant appears to argue the criticality of the process step of depositing a dielectric ARC layer on the SiNx or polysilicon layer. For support, the applicant cites the specification at page 3, line 8 through page 4, line 1. In response, the cited portion of the specification has been reviewed by the examiner. The examiner notes that the cited portion of the specification appears to teach the benefits of utilizing a dielectric ARC (SiO_2, SiON, or SiONH) instead of an organic ARC or inorganic ARC such as TiN or TiW. It does not show or suggest any criticality of either a polysilicon layer or a silicon nitride layer. Briefly, both Holscher et al. and Plat et al. are drawn to utilizing dielectric ARCs as disclosed and claimed by the applicant, not organic ARCs or inorganic ARCs such as TiN or TiW. Both are concerned with providing an effective ARC layer that can be utilized to suppress reflected radiation in later photoresist patterning procedures. Importantly, Holscher et al. teach that the semiconductive substrate on which the ARC layer is deposited includes a semiconductor wafer alone as well as assemblies comprising other materials thereon (Col.2, lines 46 – 55). Plat et al. indicate that a polysilicon layer is conventionally used on top of a semiconductor wafer in semiconductor photoresist

patterning processes such as the process of Holscher et al. As such and in view of the combined teachings of Holscher et al. and Plat et al., one of ordinary skill in the art would have clearly recognized that an "assembly" of Holscher et al. would have included a semiconductive substrate with a polysilicon layer deposited thereon. In addition, in response to the applicant's statement that neither Holscher nor Plat recognizes the criticality of a dielectric ARC layer on a surface of SiNx or polysilicon, the examiner strongly disagrees. Plat et al. explicitly teach that, in conventional semiconductor devices, an ARC layer is deposited on top of a polysilicon layer to reduce reflections that occur during a subsequent photolithography step (Col.1, lines 21 – 35, and Col.2, lines 25 – 30 and 47 – 49). This is exactly the same reason the applicant deposits the ARC layer of their invention (see page 3, line 8 to page 4, line 1 of the applicant's specification).

28. In response to the applicant's statement that neither Holscher nor Plat teaches the coating of a dielectric ARC layer of SiO_2 or SiONH, the examiner disagrees. Holscher et al. do teach an ARC layer of SiONH (Col.2, lines 56 – 67).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Foote et al. (USPN 6,365,320 B1) teach SiONH ARC layers used in semiconductor photolithography. Kim et al. (USPN 6,214,637 B1) teach annealing an ARC layer which is deposited on top of a SiN layer in order to increase the refractive index and extinction coefficient of the ARC layer (Abstract and Col.5). Holscher et al.(2)

(USPN 6,444,588 B1) teach annealing ARC layers in order to alter their optical properties.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wesley D Markham whose telephone number is (703) 308-7557. The examiner can normally be reached on Monday - Friday, 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shrive Beck can be reached on (703) 308-2333. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9310 for regular communications and (703) 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0661.

Wesley D Markham
Examiner
Art Unit 1762

WDM
December 30, 2002

MICHAEL BARR
PRIMARY EXAMINER